

in IDS filed April 26, 2002) in the rejection of claims 4-6 under § 103. Apparently, the Examiner is under the mistaken belief that because Miyazaki et al. was cited in an IDS filed after prosecution on the merits was closed, the Examiner may use Miyazaki et al. to make a new ground of rejection while maintaining the finality of the Office Action. The Examiner is directed to MPEP § 706.07(a), which sets forth the applicable standard:

second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) (emphasis added).

In the instant case, the Examiner has introduced a new ground of rejection in the outstanding Office Action with respect to claims 4-6. Specifically, in the Office Action dated April 18, 2002, the Examiner rejected claim 5 under 35 U.S.C. § 103 over APA in view of Amagai and Jiang et al., and rejected claims 4 and 6 under 35 U.S.C. § 103 over APA in view of Amagai, Jiang et al., and Lee et al.. Subsequently, in the next Office Action dated July 24, 2002, the Examiner has rejected claims 4-6 under 35 U.S.C. § 103 over APA in view of Amagai, Jiang et al., Lee et al., and Miyazaki et al.

This new ground of rejection was "neither [1] necessitated by applicant's amendment of the claims nor [2] based on information submitted in an [IDS] filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p)." With respect to the first prong, as evidenced when reviewing Applicants' response dated July 9, 2002, no amendment to the claims was made in response to the Office Action dated April 18, 2002. With respect to the second prong, the newly relied on patent to Miyazaki et al. was submitted in an IDS during the period set forth in 37 CFR 1.97(d) (i.e., NOT under 1.97(c) with payment of the fee, which would have allowed the Examiner to make the outstanding Office Action final). In other words, when using

a new reference cited in an IDS to make a new ground of rejection which is not necessitated by amendment (as in the present case), the Examiner can make the rejection final only if the IDS was submitted during the period set forth in § 1.97(c), and the fee under 1.17(p) was paid rather than making the statement under § 1.97(e). In the instant case, the IDS was filed during the period set forth in § 1.97(d), which *requires* a statement under § 1.97(e).

As can be understood by reading the pertinent sections of the MPEP, the Examiner can NOT make a rejection final which uses a newly cited reference in an IDS which is filed with a statement under § 1.97(e). The Examiner can only make a rejection final when using such a reference when it is submitted in an IDS filed during the period set forth in 1.97(c) and applicant selected to pay the fee rather than making the certification under § 1.97(e). As is apparent, applicants who just recently became aware of references cited in an IDS so as to be able to make the certification statement under § 1.97(e) are immune to final rejection using such a reference regardless of the status of prosecution (i.e., before (1.97(c)) or after final action (1.97(d))).

Based on all the foregoing, it is submitted that the finality of the outstanding Office Action is premature because the Examiner has set forth a new ground of rejection which was neither necessitated by amendment, nor based on information submitted in an information disclosure statement filed *during the period set forth in 37 CFR 1.97(c)* with the fee set forth in 37 CFR 1.17(p). Accordingly, it is requested that the finality of the outstanding Office Action be withdrawn, and for this response to be treated as a response to a non-final Office Action. It is therefore submitted that the attached amendment be entered as a matter of right, and for the amendment to be fully examined and the arguments be considered and responded to in due course.

**II. CLAIM 4 IS PATENTABLE OVER APA IN VIEW OF AMAGAI, JIANG ET AL., LEE ET AL., AND MIYAZAKI ET AL.**

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Claims 4-6 stand rejected under 35 U.S.C. § 103 over APA in view of Amagai et al., Jiang et al., Lee et al. and Miyazaki et al. This rejection is traversed for the following reasons. Applicants note that the rejection of claims 5 and 6 has been rendered moot by cancellation of the claims.

It is submitted that claim 4 is patentable based on its own merits, in addition to being dependent on novel claim 1.

**A. Proposed combination does not disclose each and every limitation**

For example, claim 4 recites in pertinent part, the *combination* of an adhesive layer which is greater in size than the primary surface of said semiconductor element and smaller in size than the primary surface of said circuit board, and which "extends radically outward relative to and completely around the primary surface of said semiconductor element." The Examiner's primary reference is APA, which the Examiner admits does not disclose an adhesive layer which is greater in size than the primary surface of the semiconductor element. As discussed in the previous response, the Examiner has effectively replaced the adhesive layer 5 of APA with the alleged adhesive layer 8 of Amagai in order to read on the limitations of claim 1.

In other words, the Examiner has already modified one time the adhesive layer of APA as the primary reference by replacing it with the adhesive layer of Amagai. As admitted by the Examiner, this combination does not disclose the limitation of claim 4. The Examiner therefore attempts to again modify the adhesive layer of Amagai in the combination of APA in view of Amagai by replacing it with the alleged adhesive layer 2 of Miyazaki et al.. As a preliminary matter, it is submitted that the alleged adhesive layer 2 of Miyazaki et al. is NOT an adhesive layer, but rather, is merely an elastomer (*see Abstract*) which is bonded to the semiconductor

chip via tape 8. Accordingly, even assuming *arguendo* that the elastomer 2 of Miyazaki et al. could somehow be incorporated into the device of APA in view of Amagai, the resulting structure would simply result in the APA device with its adhesive layer 5 sized as in Amagai, with the addition of the extra element elastomer 2 coupled to the adhesive layer 5.

Miyazaki et al. appears to be silent as to the elastomer 2 being an adhesive layer (i.e., having adhesive properties), and in fact, Miyazaki et al. appears to suggest that elastomer 2 is NOT an adhesive layer *as evidenced by the need to use tape 8, 9 to bond the elastomer 2 to the semiconductor element 1 and flexible wiring board 10, respectively*. The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claim 4 because the proposed combination fails the "all the claim limitations" standard required under § 103. In particular, the alleged adhesive layer 2 of Miyazaki et al. is NOT an adhesive layer, and assuming *arguendo* it could be properly used in the combination of APA in view of Amagai, the resulting structure would still have the same adhesive layer 5 of APA with the size of Amagai. In other words, the elastomer 2 is NOT analogous in structure or function to the adhesive layer 5 of APA in view of Amagai. Accordingly, any modification to APA/Amagai using elastomer 2 of Miyazaki et al. would embody only the addition of elastomer 2 by bonding it to the adhesive layer 5 of APA, rather than replacing the adhesive layer 5 with the elastomer 2.

#### **B. Proposed combination is improper**

**i.      improper modification of modifying reference**

Moreover, it is submitted that proposed modification set forth by the Examiner is improper because the Examiner is attempting to modify the same limitation (adhesive layer of APA) *twice* using two different references. Although it is understood that the Examiner may use as many references as possible, it is submitted that the Examiner can NOT use multiple references to modify the *same limitation*. It is submitted that such a need to provide repeated modifications of the same limitation using multiple references evidences non-obviousness of the claimed invention. For example, if a claim recites elements A, B, ... Z, an Examiner can potentially use a primary reference which discloses A while using 25 different other references to modify the primary reference to add each of the limitations B, ... Z. However, the Examiner can not use a secondary reference to modify A to include B, then use another secondary reference to modify the already modified B. As is well known in patent prosecution, such a rejection is in effect modifying a modifying reference which is too attenuated from the claimed invention to be considered *prima facie* obvious.

In the instant case, as previously discussed, the Examiner replaced the adhesive layer 5 of APA with the adhesive layer of Amagai so that the resulting combination has an adhesive layer which does extend to the outer edge of the circuit board. Thereafter, although the Examiner can rely on other references to modify other features of APA, it is submitted that the Examiner can no longer use another reference to again modify the adhesive layer because such a modification would in effect be modifying a modifying reference (adhesive layer of Amagai) rather than modifying the primary reference APA.

**ii.      No motivation for combination**

Even furthermore, there is no need, desire nor purpose for modifying APA/Amagai with Miyazaki et al. as attempted by the Examiner because the elastomer 2 is used specifically with a **flexible** circuit board 10 for the particular purpose of stabilizing the flexible structure. There is no evidence on the record that APA uses a flexible circuit board (it appears to be rigid), thereby eliminating any potential objective evidence from the prior art that would suggest the desirability of using the elastomer 2 in the device of APA. Again, absent hindsight reconstruction, there is no rationale for using an adhesive layer with the specific **dual**-size constraints (larger than semiconductor elements and smaller than circuit board) and with specific structure that the adhesive layer extends radically outward relative to and completely around the primary surface of the semiconductor element.

That is, the cited prior art does not disclose or suggest, nor provide any motivation for, the **combination** of an adhesive layer which is **both** "greater in size than the primary surface of said semiconductor element" and "extends outside an outer edge of the primary surface of said semiconductor element without reaching an outer edge of the primary surface of said circuit board" as recited in claim 1, **and** "extends radically outward relative to and completely around the primary surface of said semiconductor element." Neither APA, Amagai, nor Miyazaki et al., alone or in combination, discloses the combination of the above limitations recited in claims 1 and 4.

In fact, the Examiner does not differentiate the motivation between modifying APA/Amagai with Miyazaki et al. or Lee. Miyazaki et al. and Lee disclose different sizes for the alleged adhesive layers, and the Examiner has improperly attempted to support the modification of APA/Amagai with both teachings of the same feature using the same motivation. It is respectfully submitted that such a reasoning is improper because the Examiner can not modify

the same limitation of APA/Amagai with two different references (i.e., what adhesive layer is the final structure going to have, Miyazaki et al.'s or Lee's?). Furthermore, the Examiner's motivation is NOT supported by the prior art and is based entirely on improper hindsight reasoning. As discussed above, the asserted motivation is taken expressly from Applicants' specification, whereas the prior art is completely silent as to the benefits of having a larger adhesive layer, *let alone an adhesive layer that is sized between the circuit board and semiconductor element.*

As discussed throughout Applicants' specification, the sizing of the adhesive layer has particular advantages to the semiconductor device embodied by the present invention. Whereas, none of the cited prior art acknowledge or consider the specific problem of internal stress of the semiconductor device resulting from differing thermal expansion coefficients. Only Applicants have recognized this particular problem, and provided the means by which to solve it.

Based on all the foregoing, it is submitted that claim 4 is patentable over APA in view of Amagai, Jiang et al., Lee et al. and Miyazaki et al.. Accordingly, it is respectfully requested that the rejection of claim 4 under 35 U.S.C. § 103 over APA in view of Amagai, Jiang et al., Lee et al. and Miyazaki et al., be withdrawn.

### **III. CLAIMS 1-3 ARE PATENTABLE OVER APA IN VIEW OF AMAGAI AND JIANG ET AL.**

Claims 1-3 stand rejected under 35 U.S.C. § 103 over APA in view of Amagai and Jiang et al.. This rejection is respectfully traversed for the following reasons.

Applicants note that claim 1 is amended to include the limitation recited in claim 6 and the limitation "said semiconductor element and said circuit board directly contact each other via

the adhesive layer in order to relieve tension between said semiconductor element and said circuit board by the adhesive layer." It is believed that by this amendment, the structure of adhesive layer and the relationship between the adhesive layer, and the semiconductor element and circuit board are more clearly defined in claim 1.

In response to Applicants' arguments that Amagai does not provide any motivation for using a wider adhesive, the Examiner simply reasserts that "[i]t would be obvious to one of ordinary skill in the art to realize that such bonding layer being greater in size ... would provide improved adhesion and rigidity for the entire structure." However, this allegation does not respond to Applicants' arguments which set forth that such an increase in size would NOT increase adhesion/rigidity of the structure. The Applicants' arguments are reprinted below for the Examiner's convenience:

The Examiner has not provided any *objective* evidence *from the prior art* as to why having an adhesive layer greater in size than the semiconductor element would improve adhesion/rigidity. The adhesive layer 5 of APA is designed simply to adhere the semiconductor element 10 to the circuit board 1. Increasing the size of the adhesive layer 5 beyond the size of the semiconductor element 10 would not meaningfully improve the adhesion between the semiconductor element 10 and the circuit board 1 *because the amount of surface contact between the semiconductor element 10 and adhesive layer 5 would still be the same.*

Furthermore, as discussed above, only Applicants have discovered the specific problems associated with stress resulting from different thermal expansion coefficients. In making the proposed combination, the Examiner simply restates Applicants' rationale for inventing the novel structure of the present invention, and alleges that one of ordinary skill in the art would have known to do the same. However, the cited *prior art* does NOT even recognize the problems solved by the present invention, let alone suggest how to solve such a problem.

It is further submitted that the Examiner has NOT responded to the other arguments made in support of patentability of claims 1-3, for example, the new and unexpected results and advantages/benefits of the present invention over the cited prior art, which are reprinted below for the Examiner's convenience:

It is respectfully submitted that the Examiner's alleged motivation is derived solely from Applicants' specification and is therefore improper hindsight reasoning. For example, page 6, lines 5-11 and/or page 8, lines 24-28 describe how the area covered by the adhesive layer beyond the semiconductor element absorbs stress due to a difference in thermal expansion coefficients so that the stress exerted on the solder joints 31-32 is alleviated. Further, on page 8, Applicants disclose that because of the larger adhesive layer, "the point about which the circuit board 1 is to warp is distant from the external electrodes provided on outermost periphery of the semiconductor device" so as to alleviate the stress exerted on the solder joints 31-32, thereby improving reliability and rigidity of the device.

These technically based findings (e.g., differences in thermal expansion coefficients and warping location of circuit board) are the only evidence on the record for supporting the motivation of providing the adhesive layer having a greater size than the semiconductor element. The cited prior art does not acknowledge nor consider such findings, and there is no objective evidence on the record that the prior art suggests the desirability of having a larger adhesive layer. Again, at best, the Examiner has attempted to show only that the elements of the claimed invention are *individually* known without providing a *prima facie* showing of obviousness that the *combination* of elements recited in claim 1 is known or suggested in the art. It is respectfully submitted that the Examiner has selected bits and pieces of the cited prior art and relied solely on improper hindsight reasoning using only Applicants' specification as a guide to reconstruct the claimed invention.

If the Examiner maintains the pending rejection, it is respectfully requested that he provide some *objective* technical evidence *from the prior art* (i.e., independent of Applicants' specification) that supports his allegation that the motivation for modifying APA with Amagai is suggested by the prior art rather than Applicants' specification.

Furthermore, it is submitted that the present invention provides new and unexpected results over the device of the proposed combination of references. As such, it is submitted that the proposed combination would not have been obvious to one of ordinary skill in the art (absent hindsight reasoning) because the claimed invention improves upon known devices by correcting a problem previously undealt with in the prior art. That is, the *combination* of elements recited in claims 1-3, even assuming *arguendo* they are known[n] *individually* in the art, provide certain advantages and benefits as a combination that are both new and unexpected over existing devices.

Accordingly, it is submitted that these differences between the prior art and the present invention emphasize the non-obviousness of the *combination* of elements recited in claims 1-3, so as to effectively render the proposed combination of APA, Amagai and Jiang et al. improper. Specifically, none of the cited prior art recognizes or attempts to solve the interface problem between the adhesive layer and molding resin which leads to undesirable moisture absorption and high temperature deterioration.

In particular, when the adhesive layer extends up to the periphery of the substrate as in the proposed combination set forth by the Examiner (i.e., where the APA adhesive layer is replaced with the Amagai adhesive layer), the interface between the adhesive layer and the molding resin may tend to tear, and moisture absorption or high temperature deterioration might be caused. In contrast, in the present invention, the peripheral region of the substrate can be covered by the molding resin *in combination* with an adhesive layer which is larger than the semiconductor element, so that the above characteristics are improved and the benefits of both features can be obtained in a single device. None of the cited prior art discloses or suggests such a combination, let alone recognize or appreciate the dual benefits derived therefrom. Accordingly, the present invention provides a device which is superior to known prior art devices, rendering any combination of references to reach such a construction as non-obvious. In general, an adhesive layer tends to absorb moisture than a molding resin, i.e., Tg (glass transformation temperature) is low. Additionally, in the proposed combination, the chip is provided via an elastomer layer on a flexible substrate, whereas in the present invention the chip can be provided on a rigid substrate so as to further improve the characteristics of the device.

The Examiner is directed to MPEP § 2143.01 under the subsection entitled "Fact that the Claimed Invention is Within the Capabilities of One of Ordinary Skill in the Art is Not Sufficient by Itself to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

A statement that modifications of the prior art to meet the claimed invention would have been [obvious] because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. (citing *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)).

In the instant case, even assuming *arguendo* that APA and Amagai "teach that all aspects of the claimed invention [are] individually known in the art", it is submitted that such a conclusion "is not sufficient to establish a *prima facie* case of obviousness" because there is no objective reason on the record to combine the teachings of the cited prior art in the manner set forth by the Examiner. As discussed above, neither APA nor Amagai disclose or suggest an adhesive layer

having a "middle" size which is larger than the semiconductor element but smaller than the circuit board.

At best, the Examiner has attempted to show only that the elements of the claimed invention are *individually* known (i.e., adhesive layer which is larger than semiconductor element **OR** adhesive layer smaller than circuit board) without providing a *prima facie* showing of obviousness that the *combination* of elements (i.e., adhesive layer which is larger than semiconductor element **AND** adhesive layer smaller than circuit board) recited in claim 1 in combination with claim 5, is known or suggested in the art. It is respectfully submitted that the Examiner has selected bits and pieces of the cited prior art and relied solely on improper hindsight reasoning using only Applicants' specification as a guide to reconstruct the claimed invention.

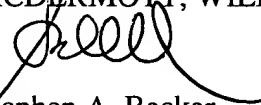
Based on all the foregoing, it is submitted that claims 1-3 are patentable over APA in view of Amagai and Jiang et al.. Accordingly, it is respectfully requested that the rejection of claims 1-3 under 35 U.S.C. § 103 over APA in view of Amagai and Jiang et al., be withdrawn.

### CONCLUSION

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,  
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## APPENDIX

### IN THE CLAIMS:

1. (Amended) A semiconductor device comprising:

a semiconductor element having a primary surface and a back surface, said semiconductor element having an element electrode on the primary surface; and a circuit board having a primary surface and a back surface, said circuit board having a board electrode on at least the back surface, said circuit board having a predetermined opening hole formed therein;

wherein the primary surface of said semiconductor element is bonded to the primary surface of said circuit board by means of an adhesive layer which is greater in size than the primary surface of said semiconductor element, [and]

said adhesive layer extends outside an outer edge of the primary surface of said semiconductor element without reaching an outer edge of the primary surface of said circuit board,

    said element electrode of said semiconductor element is connected to said board electrode provided on the back surface of said circuit board via said opening hole, and

said semiconductor element and said circuit board directly contact each other via the adhesive layer in order to relieve tension between said semiconductor element and said circuit board by the adhesive layer.

4. (Amended) The semiconductor device according to claim 1, wherein said adhesive layer [includes a portion which] extends radically outward relative to and completely

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around the primary surface of said semiconductor element[, said portion extending completely around the primary surface of said semiconductor element].